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Abdelouahab BENTRCIA

Thème

Les Structures d'Annulation Linéaire d'Interférence Dans les Systèmes Cellulaires DS-CDMA

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Devant la commission d'examen composée de:

Mohamed Boulemden	Professeur	Université de Batna	Président
Moussa Benyoucef	Maître de conférences	Université de Batna	Rapporteur
Azzedine Zerguine	Professeur Associé	Université Roi Fahd du Pétrole et des minéraux (KFUPM)	Rapporteur (à l'étranger)
Faouzi Soltani	Professeur	Université de Constantine	Examinateur
Djamel Chikouche	Professeur	Université de M'sila	Examinateur
Lamir Saidi	Maître de conférences	Université de Batna	Examinateur

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Abdelouahab

Abstract

The main goal of this dissertation is to investigate linear interference cancellation structures that are appropriate for long-code CDMA systems. Motivated by the lack of such structures and exploiting the fact that for long-code CDMA systems, the major computational complexity burden comes from the frequent calculation of the cross- correlation matrix (it should be calculated each symbol period) and not from the interference cancellation itself, we examine the possibility of developing interference cancellation schemes that avoid the calculation of the cross-correlation matrix. Such structures are known as chip-level (wideband) interference cancellation schemes and they directly make use of the spreading codes instead of the cross-correlation coefficients, hence the additional burden of the cross-correlation computation is avoided. Our approach for developing such structures is based on the equivalence between some of the chip-level linear interference cancellation structures and linear iterative methods. Such mapping will not only enable the identification of new interference cancellation schemes that correspond to other iterative methods but will also facilitate the study of the convergence behavior of these structures based on the rich theory developed within the frame of iterative methods. In chapter 8, two new chip-level linear weighted SIC/weighted group-wise SIC structures that can converge not only to the decorrelator detector but also to the LMMSE detector are derived. They proved to exhibit less computational complexity than their symbol-level counterparts. In chapter 9, four novel chip-level linear weighted SIC/weighted group-wise SIC structures that are equivalent to linear SOR/linear BSOR iterative methods are derived. Their convergence behavior is analyzed and their conditions of convergence are determined using two different methods that lead to the same result. In chapter 10, using a matrix iterative analysis approach, the chip-level linear group-wise structure is shown to be equivalent to the linear BSOR iterative method but with a relaxation matrix rather than a relaxation factor. Establishing such connection allows the proposition of two new corollaries from which two conditions of convergence are determined. In chapter 11, a new chip-level linear group-wise PIC detector is proposed. Its inherent parallelism facilitates its implementation in a parallel multiprocessor structure and reduces considerably the algorithm time complexity. Other by-product contributions are also obtained in chapters 4, 5 and 7 respectively.

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