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Proceedings

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F. Makedon, K. Mehlhorn, T. Papatheodorou and P. Spirakis

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FOREWORD

The papers in this volume were presented at the *Aegean Workshop on Computing: VLSI Algorithms and Architectures (AWOC 86)*, organized by the Computer Technology Institute in Patras in cooperation with ACM, EATCS, IEEE and the General Secretariat of Research and Technology (Ministry of Industry, Energy & Technology of Greece). They were selected from 70 abstracts submitted in response to the program committee's call for papers. We thank all those who submitted abstracts for their interest in AWOC. We expect that revised and expanded versions of many of the submissions will eventually appear in refereed journals.

AWOC 86 will take place in Loutraki, Greece, July 8-11, 1986. AWOC 86 is the second meeting in the *International Workshop on Parallel Computing & VLSI* series; the first meeting took place in Amalfi, Italy, 1984.

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DIGITAL FILTERING IN VLSI[+]

G. Bilardi* and F.P. Preparata**

(Invited Paper)

Abstract: In this paper we take a first step in the study of VLSI realizations of digital filtering. For increasing input rate, processing is feasible only by resorting to massive parallelism, i.e., to an nq-th extension of the original order-n filter. We show that the operation is reducible to convolutions with fixed n-vectors and propose to realize the computation by means of the twisted-reflected-tree, a network naturally suited for prefix computation. We discuss the issues of precision and operand length, and illustrate the arising area/data-rate/delay trade-offs.

1. Introduction

Digital signal processing is one of the most important special-purpose computations. Although a primary target of VLSI implementation, this problem has not yet been analyzed - except for preliminary attempts - in the context of VLSI computation theory. The purpose of this paper is to take a first step in such analysis.

In recent years, a *VLSI model of computation* has been proposed ([T80], [BK81]) to capture the essential features of VLSI as a computing environment and to allow for mathematical analysis of chip design. The performance of designs has generally been measured in terms of the chip area A, and of the computation time T. The area-time trade-off has been investigated for several fundamental computational problems.

In this context, two basic operations of signal processing have received considerable attention: *convolution* [BPV83], and *discrete Fourier transform* ([T80], [PV81], [T83], [BS84]). In this paper we begin to investigate, from the VLSI complexity perspective, the central problem of digital signal processing, that is *digital filtering*.

A *digital filter* (of order n) is a length-preserving transducer whose input and output are discrete-time signals related by an n-th order linear constant coefficient difference equation [OS75], [K80]. Since the input and the output of the filter are infinite sequences, a computation time relative to the entire input is meaningless in this context. Instead, the following measures are of interest: the *data rate*, ρ, defined as the number of input samples received per unit time, and the *delay*, Δ, defined as the (maximum of the) difference between the time at which a given output sample is produced and the time at which the corresponding input sample is read. We shall therefore study the area/data-rate/delay trade-off of VLSI digital filters, as a function of the order of the filter and of the precision by which signal samples are represented.

Traditional structures for filters ([OS75], Chapter 4) are interconnections of adders, multipliers, and delay elements. Typically, signal samples are input one at a time, and the period between consecutive samples is at least of the order of one multiplication time. The area/data-rate trade-off of these structures is due only to the area-time trade-off of their arithmetic components, and the maximum data rate is limited by the maximum speed at which numbers of the desired precision can be multiplied.

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Here we propose a new algorithm for filtering that, by working on a multiplexed version of the input signal, can process many samples simultaneously. The data rate can be increased without changing the speed of the basic arithmetic blocks, obviously at the expense of a higher degree of parallelism in the system, and therefore of a larger area.

In Section 2 we obtain an interesting expression of the input-output relation of an n-th order filter in terms of convolutions of sequences of $O(n)$ length. In Section 3 we propose an implementation of the digital filter as a network of convolvers. In Section 4, we determine the operand length required to achieve the desired precision. Finally, in Section 5, the area/data-rate/delay trade-off of this network is discussed for the case in which the convolver structure of [BPV83] is deployed.

2. Problem Formulation

A digital filter is a linear time-invariant system described by the difference equation

$$\sum_{j=0}^{n} a_j\, y(t-j) = \sum_{i=0}^{n-1} b_i\, u(t-i) \tag{1}$$

where $u(t)$ (the input signal) and $y(t)$ (the output signal) are real-valued functions of the integer variable t (time), and the a_i's and b_j's (the filter coefficients) are real constants with $a_0 = 1$.

It is convenient to consider a state-variable representation of filter (1) of the type

$$\mathbf{x}(t+1) = \mathbf{A}\,\mathbf{x}(t) + \mathbf{b}\,u(t), \tag{2}$$

$$y(t) = \mathbf{c}^T \mathbf{x}(t) + d\,u(t), \tag{3}$$

where $\mathbf{x}(t)$ is an n-dimensional state vector, $\mathbf{A}$ an $n \times n$ matrix (transition matrix), $\mathbf{b}$ and $\mathbf{c}$ n-dimensional vectors, and d a scalar. Among the quadruples $(\mathbf{A}, \mathbf{b}, \mathbf{c}, d)$ that make (2) and (3) a realization of (1), we choose the one known as *reachability form* where $\mathbf{A}$ [K80, p.95] is the companion matrix with last row $[-a_n, \ldots, -a_1]$, $\mathbf{b} \triangleq [0, \ldots, 0, 1]^T$, $\mathbf{c} \triangleq [(b_n - b_0 a_n), \ldots, (b_1 - b_0 a_1)]^T$, and $d \triangleq b_0$. We also introduce the reachability matrix $\mathbf{R} = [\mathbf{A}^{n-1}\mathbf{b}, \mathbf{A}^{n-2}\mathbf{b}, \ldots, \mathbf{b}]$ and the observability matrix $\mathbf{H} = [\mathbf{c}, \mathbf{A}^T\mathbf{c}, \ldots, (\mathbf{A}^T)^{n-1}\mathbf{c}]^T$ associated with representation (2) and (3) [K80, p.80].

We now consider the n-th order extension of filter (1), with input $\mathbf{u}(t) = [u(t), u(t+1), \ldots, u(t+n-1)]^T$, output $\mathbf{y}(t) = [y(t), y(t+1), \ldots, y(t+n-1)]^T$, and state $\mathbf{x}(t)$. Repeated application of (2) and (3) yields the following equations for the extension:

$$\mathbf{x}(t+n) = \mathbf{F}\,\mathbf{x}(t) + \mathbf{R}\,\mathbf{u}(t), \tag{4}$$

$$\mathbf{y}(t) = \mathbf{H}\,\mathbf{x}(t) + \mathbf{T}\,\mathbf{u}(t), \tag{5}$$

where $\mathbf{F} \triangleq \mathbf{A}^n$, and $\mathbf{T}$ is a lower-triangular $n \times n$ Toeplitz matrix with first column $[d, \mathbf{c}^T\mathbf{b}, \mathbf{c}^T\mathbf{A}\mathbf{b}, \ldots, \mathbf{c}^T\mathbf{A}^{n-2}\mathbf{b}]^T$.

The following lemmas show that the matrices $\mathbf{F}$, $\mathbf{R}$, $\mathbf{H}$, and $\mathbf{T}$ have a special structure that can be exploited when computing $\mathbf{x}(t+n)$ and $\mathbf{y}(t)$ via (4) and (5).

Lemma 1. Let r_j, $-\infty < j < +\infty$, be the solution of the equation $r_j + a_1 r_{j-1} + \ldots + a_n r_{j-n} = 0$, such that $r_0 = 1$ and $r_j = 0$ for $j < 0$. Let $\mathbf{R}_j$ denote the Toeplitz matrix

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