IEEE INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

ICCAD-87

A CONFERENCE FOR THE EE CAD PROFESSIONAL

NOVEMBER 9-12, 1987
CONVENTION CENTER
SANTA CLARA, CALIFORNIA

IEEE

DIGEST OF TECHNICAL PAPERS

Sponsored by
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In Cooperation with
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Association for Computing Machinery

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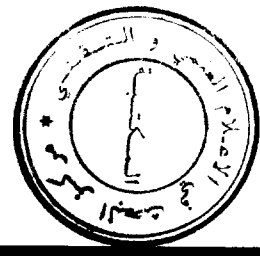

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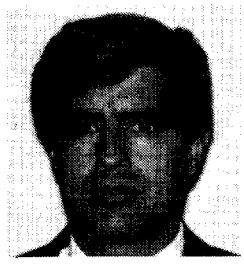
Foreword



On behalf of the Conference Executive Committee, it is our pleasure to welcome the participants to ICCAD-87, the 5th IEEE International Conference on Computer-Aided Design. The members of the Conference Executive Committee and the Technical Program Committee have strived to maintain the tradition of excellence set in the previous conferences. We hope that the conference will meet your objectives and expectations.

This year, a record number of papers were submitted to the Technical Program Committee. Four hundred forty papers from 28 countries were received. Of these, 171 were received from outside of the United States, illustrating the true international nature of the conference. Likewise, there was a good blend of papers received from industry and universities.

The submitted papers were reviewed intensively by members of the Technical Program Committee, which was subdivided into four subcommittees: Simulation, Layout, Test and Systems. Each subcommittee consisted of 10 members, including two from outside of the United States. The members of the Technical Program Committee have selected 119 papers for presentation at the conference in 35 sessions. Since the length of the papers in the Digest was limited to four pages, all authors are being encouraged to submit expanded versions to the *IEEE Transactions on CAD/ICAS*, the *IEEE Design and Test* magazine, the *IEEE Circuits and Device* magazine, the *ACM SIGMA Newsletter*, or other similar publications.

As in previous years, the conference will include tutorials and a workshop on Monday, followed by technical presentations Tuesday through Thursday. Two panel sessions will be held on Tuesday evening, and a banquet will be held on Wednesday evening to facilitate honors on recipients of various awards from the sponsoring IEEE Societies: the IEEE Circuits and Systems Society and the Computer Society of the IEEE. This year's banquet speaker is Dr. R. J. Herfkens, who will speak on the application of computer-aided imaging techniques in the field of medical diagnosis.

Thank you for participating.

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Tutorial: Introduction to Circuit Simulation

Jacob White, MIT, Cambridge, MA

Because of the enormous cost of integrated circuit fabrication, most circuit designers use a variety of simulation tools to try to detect design errors before fabrication. The most general and reliable technique for performing this kind of simulation is to construct a system of nonlinear differential equations that describe a given circuit, and to solve the differential equation system numerically. This is referred to as circuit simulation, and by far the most popular circuit simulation program is SPICE.

In this tutorial, we will present a basic introduction to the algorithms used in programs like SPICE: circuit equation formulation, nonlinear system solution algorithms, sparse matrix techniques, and numerical integration methods. We will then examine three topics chosen from current research in circuit simulation: speedups obtained from specialized algorithms for MOS digital circuits, including relaxation techniques; parallel approaches to circuit simulation that can exploit new multiprocessor systems; and nonlinear frequency domain analysis.

Tutorial: Artificial Intelligence Applications for Test Generation

Narinder Singh, Stanford University, Stanford, CA
Mark Shirley, MIT, Cambridge, MA

This tutorial will present a detailed description of the current work in Artificial Intelligence (AI) applied to test generation. The test generation techniques discussed are device independent (general), and do not rely on any structured design techniques (e.g., scan path, LSSD).

The tutorial will begin with a description of AI techniques for knowledge representation and reasoning, which are suitable for encoding declarative (explicit) descriptions of devices. We will next present a device independent test generation system which generates tests by propagating symbolic values forward and backward through a hierarchical design. This will be followed by a description of a complementary approach which uses symbolic simulation techniques to cache controllability and observability information, which is later used in the test generation process. We will also discuss testing-cliches, and the relationship of these testing methods to design for testability, diagnosis and verification.

Tutorial: Logic Synthesis

Jeffrey R. Fox, SILC Technologies, Inc., Waltham, MA

In this tutorial we will learn how new computer programs performing logic synthesis can bridge the gap between high-level behavioral specifications and lower-level structural domains. These programs assume responsibility for the detailed logic design, freeing the designer to innovate at the behavioral and architectural levels.

The components of a logic synthesis system will be discussed including: computational models, behavioral-level hardware description languages, functional simulation, resource allocation and optimization, two-level and multi-level Boolean logic minimization, and technology binding. Particular attention will be paid to logic synthesis with timing and area constraints. The link to specific physical implementation strategies will be explored, including the relationship between logic synthesis, semi-custom VLSI, and silicon compilation. The tutorial will conclude with a detailed example and a discussion of the direction and challenges of logic synthesis research.

Tutorial: VHDL

Rick Miller, AFWAL/AADE-3, Wright Patterson Air Force Base, OH

Hardware description languages are crucial in the specification, design, verification and fabrication of electronic systems. Unfortunately, current tools make thoroughly documenting a complex, integrated system composed of many VLSI components a difficult if not impossible task. This tutorial will examine the U. S. Department of Defense's VHSIC Hardware Description Language (VHDL), IEEE proposed standard 1076/b, and its impact on the design field.

After presenting a short VHDL tutorial, the session will concentrate on CAD tools currently under development that support or utilize the VHDL. Emphasis will be given to tools that provide a direct route to silicon production. No prior knowledge of the Department of Defense's VHSIC program or the VHDL is required. Throughout the course of the day, audience participation will be encouraged.

Workshop: EDIF

Mike Waters, Motorola, Inc., Mesa, AR

Spanning the chasm that a design must cross to become silicon, the Electronic Design Interchange Format (EDIF) is gaining industry acceptance as a standard means of exchanging design information. Foundry-to-designer and designer-to-foundry communications may be conducted entirely in EDIF, conveying required data in a language understood by all.

The workshop, after presenting a brief history and an overview of the language, will concentrate on the current version of EDIF: its applications, limitations, and possible courses of future evolution. Throughout the course of the day, active audience participation will be encouraged.

Participants should be familiar with EDIF prior to attending this workshop.

Panel Session 1: Is Simulated Annealing Practical for CAD?

Jonathan Allen, MIT (Moderator)
Vishwani Agrawal, AT&T Bell Laboratories
C. L. Liu, University of Illinois
Alberto Sangiovanni-Vincentelli, University of California, Berkeley
Eugene Shragowitz, University of Minnesota
Jiri Soukup, SDA Systems
Kazuhiro Ueda, NTT

In this panel, simulated annealing approaches to the development of several CAD tools will be described together with an assessment of the results. This approach will be compared with other techniques and future directions will be projected.

Panel Session 2: Mixed Digital/Analog Simulation: Its Glories and Its Ghosts

Paul Weil, Silvar-Lisco, Inc. (Moderator)
Hugo De Man, IMEC
A. Richard Newton, University of California, Berkeley
Ronald Rohrer, Carnegie Mellon University
David Smith, Analogy, Inc.

Its glory is simultaneous digital and analog simulation with accuracy concentrated where you need it. The ghosts are multiple levels of modeling complexity with large simulator overhead and balancing. The desire is a solution to a digital problem but all the time is spent in the analog portion.

Acknowledgements

The Executive Committee of ICCAD-87 would like to extend its deepest gratitude to the following persons for all efforts on behalf of the Conference and its publications:

Linda Nemeth (AT&T Bell Laboratories)	Provided secretarial help to the Conference Chairperson.
Suzanne Kinner (Mentor Graphics Corporation)	Handled the manuscript receipt and recording procedures for over 440 submissions, and communicated with authors.
Kathy Samudovsky (Carnegie Mellon University)	Assisted in the editing and composing of text and produced camera-ready copy for the Advance and Final Programs.
Pat Pistilli (MP Associates)	Assisted with the production of the Advance and Final Programs.
Wendy Rochelle & Glenda McBride (Computer Society)	Coordinated the production of the Advance Program.
Denise Felix (Computer Society)	Coordinated the production of the Digest, and the mailing of authors' kits.

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