Dynamic Clock Stretching for Variation Compensation in VLSI Circuit Design

VENKATARAMAN MAHALINGAM, Texas Instruments
NAGARAJAN RANGANATHAN and RANSFORD HYMAN JR., University of South Florida

16

In the nanometer era, process, voltage, and temperature variations are dominating circuit performance, power, and yield. Over the past few years, statistical optimization methods have been effective in improving yield in the presence of uncertainty due to process variations. However, statistical methods overconsume resources, even in the absence of variations. Hence, to facilitate a better performance-power-yield trade-off, techniques that can dynamically enable variation compensation are becoming necessary. In this article, we propose a dynamic technique that controls the instance of data capture in critical path memory flops, by delaying the clock edge trigger. The methodology employs a dynamic delay detection circuit to identify the uncertainty in delay due to variations and stretches the clock in the destination flip-flops. The delay detection circuit uses a latch and set of combinational gates to dynamically detect and create the slack needed to accommodate the delay due to variations. The Clock Stretching Logic (CSL) is added only to paths, which have a high probability of failure in the presence of variations. The proposed methodology improves the timing yield of the circuit without significant overcompensation. The methodology approach was simulated using Synopsys design tools for circuit synthesis and Cadence tools for placement and routing of the design. Extraction of parasitic of timing information was parsed using Perl scripts and simulated using a simulation program generated in C++. Experimental results based on Monte-Carlo simulations on benchmark circuits indicate considerable improvement in timing yield with negligible area overhead.

Categories and Subject Descriptors: C.4.5 [**Performance of Systems**]: Reliability, availability, and serviceability

General Terms: Design, Reliability, Performance

Additional Key Words and Phrases: Proces variations, clock, performance

ACM Reference Format:
Mahalingam, V., Ranganathan, N., and Hyman, Jr., R. 2012. Dynamic clock stretching for variation compensation in VLSI circuit design. ACM J. Emerg. Technol. Comput. Syst. 8, 3, Article 16 (August 2012), 13 pages.
DOI = 10.1145/2287696.2287699 http://doi.acm.org/10.1145/2287696.2287699

1. INTRODUCTION

Technology scaling into the nanometer dimensions has made the design of high-performance and versatile computing systems feasible. Smaller feature size of devices

This article is an extended version of Mahalingam et al [2010] reported in *Proceedings of the International Symposium on Electronic System Design*, pp. 125–130.
This research is supported in part by a grant from Semiconductor Research Corporation (SRC) under the contract 2007-HJ-1596 and by National Science Foundation (NSF) Computing Research Infrastructure grant CNS-0551621.
Authors' addresses: V. Mahalingam, Texas Instruments, Dallas, TX; N. Ranganathan (corresponding author) and R. Hyman, Jr., Computer Science and Engineering Department, University of South Florida; email: ranganat@cse.usf.edu.

DOI 10.1145/2287696.2287699 http://doi.acm.org/10.1145/2287696.2287699