

September 11–15, 2010
Vienna, Austria



Association for
Computing Machinery

Advancing Computing as a Science & Profession



PACT'10

Proceedings of the Nineteenth International Conference on
Parallel Architectures and Compilation Techniques

Sponsored by:

ACM SIGARCH, IEEE TCPP and TCCA, and IFIP WG10.3

Supported by:

**AMD, Hewlett-Packard, IBM, IBM Research, Intel, NSF, Power.org,
Qualcomm, Reservoir Labs, and City of Vienna**

Table of Contents

PACT 2010 Conference Organization	xiii
--	-------------

PACT 2010 Sponsors & Supporters	xviii
--	--------------

Keynote Address I

Session Chair: Michael Gschwind (*IBM Systems and Technology Group*)

- **Build Watson: An Overview of DeepQA for the Jeopardy! Challenge** 1
David Ferrucci (*IBM Research*)

Keynote Address II

Session Chair: Valentina Salapura (*IBM T.J. Watson Research Center*)

- **Towards a Science of Parallel Programming** 3
Keshav Pingali (*The University of Texas at Austin*)

Keynote Address III

Session Chair: Jens Knoop (*Technische Universität Wien*)

- **Raising the Level of Many-Core Programming
with Compiler Technology — Meeting a Grand Challenge** 5
Wen-mei Hwu (*University of Illinois at Urbana-Champaign*)

Session 1A: Power-Aware Design

Session Chair: Sandhya Dwarkadas (*University of Rochester*)

- **Power and Thermal Characterization of POWER6 System** 7
Victor Jiménez, Francisco J. Cazorla, Roberto Gioiosa, Mateo Valero (*Barcelona Supercomputing Center*),
Carlos Boneti (*Schlumberger BRGC*),
Eren Kursun, Chen-Yong Cher, Canturk Isci, Alper Buyuktosunoglu, Pradip Bose (*IBM T.J. Watson Research Center*)
- **System-Level Max Power (SYMPO) — A Systematic Approach
for Escalating System-Level Power Consumption Using Synthetic Benchmarks** 19
Karthik Ganesan, Jungho Jo, W. Lloyd Bircher, Dimitris Kaseridis, Zhibin Yu,
Lizy K. John (*University of Texas at Austin*)
- **Scalable Thread Scheduling and Global Power Management
for Heterogeneous Many-Core Architectures** 29
Jonathan A. Winter (*Google Inc.*), David H. Albonesi, Christine A. Shoemaker (*Cornell University*)
- **Dynamically Managed Multithreaded Reconfigurable Architectures
for Chip Multiprocessors** 41
Matthew A. Watkins, David H. Albonesi (*Cornell University*)

Session 1B: Analysis & Optimization

Session Chair: Andreas Krall (*Technische Universität Wien*)

- **Accelerating Multicore Reuse Distance Analysis with Sampling and Parallelization** 53
Derek L. Schuff, Milind Kulkarni, Vijay S. Pai (*Purdue University*)
- **Simple and Fast Biased Locks** 65
Nalini Vasudevan (*Columbia University*), Kedar S. Namjoshi (*Bell Laboratories*),
Stephen A. Edwards (*Columbia University*)
- **Avoiding Deadlock Avoidance** 75
Hari K. Pyla, Srinidhi Varadarajan (*Virginia Polytechnic Institute and State University*)
- **DAFT: Decoupled Acyclic Fault Tolerance** 87
Yun Zhang (*Princeton University*), Jae W. Lee (*Parakinetix Inc.*),
Nick P. Johnson, David I. August (*Princeton University*)

Session 2A: Caches & Coherence I

Session Chair: Pedro Trancoso (*University of Cyprus*)

- **WAYPOINT: Scaling Coherence to 1000-Core Architectures** 99
John H. Kelm, Matthew R. Johnson, Steven S. Lumetta,
Sanjay J. Patel (*University of Illinois at Urbana-Champaign*)
- **Subspace Snooping: Filtering Snoops with Operating System Support** 111
Daehoon Kim, Jeongseob Ahn, Jaehong Kim, Jaehyuk Huh (*Korea Advanced Institute of Science & Technology*)
- **Proximity Coherence for Chip Multiprocessors** 123
Nick Barrow-Williams (*University of Cambridge*), Christian Fensch (*University of Edinburgh*),
Simon Moore (*University of Cambridge*)
- **SPACE: Sharing Pattern-Based Directory Coherence for Multicore Scalability** 135
Hongzhou Zhao, Arvindh Shriraman, Sandhya Dwarkadas (*University of Rochester*)

Session 2B: Parallelization and Parallel Programming I

Session Chair: Rudolf Eigenmann (*Purdue University*)

- **Feedback-Directed Pipeline Parallelism** 147
M. Aater Suleman (*The University of Texas at Austin*),
Moinuddin K. Qureshi (*IBM T.J. Watson Research Center*),
Khubaib, Yale N. Patt (*The University of Texas at Austin*)
- **Scalable Hardware Support for Conditional Parallelization** 157
Zheng Li (*INRIA Saclay*), Olivier Certner (*ST Microelectronics & INRIA Saclay*),
Jose Duato (*Polytechnic University of Valencia*), Olivier Temam (*INRIA Saclay*)
- **Reducing Task Creation and Termination Overhead in Explicitly Parallel Programs** 169
Jisheng Zhao, Jun Shirako (*Rice University*), V. Krishna Nandivada (*IBM India Research Laboratory*),
Vivek Sarkar (*Rice University*)
- **MEDICS: Ultra-Portable Processing for Medical Image Reconstruction** 181
Ganesh Dasika, Ankit Sethia, Vincentius Robby, Trevor Mudge, Scott Mahlke (*University of Michigan*)

Session 3A: Heterogeneous Platforms and Frameworks

Session Chair: Calin Cascaval (*Qualcomm Research*)

- **An OpenCL Framework for Heterogeneous Multicores with Local Memory** 193
Jaejin Lee, Jungwon Kim, Sangmin Seo, Seungkyun Kim, Jungho Park, Honggyu Kim, Thanh Tuan Dao,
Yongjin Cho (*Seoul National University*), Sung Jong Seo, Seung Hak Lee, Seung Mo Cho, Hyo Jung Song,
Sang-Bum Suh, Jong-Deok Choi (*Samsung Electronics Company*)
- **Twin Peaks: A Software Platform for Heterogeneous Computing on General-Purpose and Graphics Processors** 205
Jayanth Gummaraju, Laurent Morichetti, Michael Houston, Ben Sander,
Benedict R. Gaster, Bixia Zheng (*Advanced Micro Devices Inc.*)
- **MapCG: Writing Parallel Program Portable Between CPU and GPU** 217
Chuntao Hong, Dehao Chen, Wenguang Chen, Weimin Zheng (*Tsinghua University*),
Haibo Lin (*China Research Laboratory of IBM*)
- **Adaptive Spatiotemporal Node Selection in Dynamic Networks** 227
Pradip Hari, John B. P. McCabe, Jonathan Banafato, Marcus Henry (*Rutgers University*), Kevin Ko, Emmanouil
Koukoudidis (*Princeton University*), Ulrich Kremer (*Rutgers University*),
Margaret Martonosi (*Princeton University*), Li-Shiuan Peh (*Massachusetts Institute of Technology*)

Session 3B: Scheduling and Design Optimization

Session Chair: Antonia Zhai (*University of Minnesota*)

- **On Mitigating Memory Bandwidth Contention Through Bandwidth-Aware Scheduling** 237
Di Xu, Chenggang Wu (*Chinese Academy of Sciences*),
Pen-Chung Yew (*University of Minnesota at Twin-Cities & Academia Sinica, Taiwan*)
- **AKULA: A Toolset for Experimenting and Developing Thread Placement Algorithms on Multicore Systems** 249
Sergey Zhuravlev, Sergey Blagodurov, Alexandra Fedorova (*Simon Fraser University*)

- **Criticality-Driven Superscalar Design Space Exploration**261
Sandeep Navada, Niket K. Choudhary, Eric Rotenberg (*North Carolina State University*)
- **A Programmable Parallel Accelerator for Learning and Classification**273
Srihari Cadambi, Abhinandan Majumdar, Michela Becchi, Srmat Chakradhar,
Hans Peter Graf (*NEC Laboratories America, Inc.*)

Session 4: Best Papers

Session Chairs: Michael Gschwind (*IBM Systems and Technology Group*),
Jens Knoop (*Technische Universität Wien*)

- **Discovering and Understanding Performance Bottlenecks in Transactional Applications**285
Ferah Zylkyarov, Srdjan Stipic (*BSC-Microsoft Research Centre & Universitat Politècnica de Catalunya*),
Tim Harris (*Microsoft Research*), Osman S. Unsal (*BSC-Microsoft Research Centre*),
Adrián Cristal (*BSC-Microsoft Research Centre, IIIA - Artificial Intelligence Research Institute CSIC - Spanish National Research Council*), Ibrahim Hur (*BSC-Microsoft Research Centre*),
Mateo Valero (*BSC-Microsoft Research Centre, Universitat Politècnica de Catalunya*)
- **Efficient Sequential Consistency Using Conditional Fences**295
Changhui Lin (*University of California, Riverside*), Vijay Nagarajan (*University of Edinburgh*),
Rajiv Gupta (*University of California, Riverside*)
- **Partitioning Streaming Parallelism for Multi-Cores: A Machine Learning Based Approach**307
Zheng Wang, Michael F. P. O'Boyle (*The University of Edinburgh*)
- **Handling the Problems and Opportunities Posed by Multiple On-Chip Memory Controllers**319
Manu Awasthi, David Nellans, Kshitij Sudan, Rajeev Balasubramonian, Al Davis (*University of Utah*)

Session 5A: Languages and Compilers

Session Chair: Vivek Sarkar (*Rice University*)

- **Design and Implementation of the PLUG Architecture for Programmable and Efficient Network Lookups**331
Amit Kumar, Lorenzo De Carli, Sung Jin Kim, Marc de Kruijf,
Karthikeyan Sankaralingam (*University of Wisconsin-Madison*),
Cristian Estan (*NetLogic Microsystems*), Somesh Jha (*University of Wisconsin-Madison*)
- **A Model for Fusion and Code Motion in an Automatic Parallelizing Compiler**343
Uday Bondhugula, Oktay Gunluk, Sanjeeb Dash,
Lakshminarayanan Renganarayanan (*IBM T.J. Watson Research Center*)
- **Ocelot: A Dynamic Optimization Framework for Bulk-Synchronous Applications in Heterogeneous Systems**353
Gregory Diamos, Andrew Kerr, Sudhakar Yalamanchili, Nathan Clark (*Georgia Institute of Technology*)
- **An Empirical Characterization of Stream Programs and Its Implications for Language and Compiler Design**365
William Thies (*Microsoft Research India*), Saman Amarasinghe (*Massachusetts Institute of Technology*)

Session 5B: ACM Student Research Competition

Session Chairs: M. Anton Ertl & Franz Puntigam (*Technische Universität Wien*)

Session 6A: Parallelization and Parallel Programming II

Session Chair: David Gregg (*Trinity College Dublin*)

- **Semi-Automatic Extraction and Exploitation of Hierarchical Pipeline Parallelism Using Profiling Information**377
Georgios Tournavitis, Björn Franke (*University of Edinburgh*)
- **The Parallax Infrastructure: Automatic Parallelization with a Helping Hand**389
Hans Vandierendonck, Sean Rul, Koen De Bosschere (*Ghent University*)

- **AM++: A Generalized Active Message Framework**401
Jeremiah J. Willcock (*Indiana University*), Torsten Hoefer (*University of Illinois at Urbana-Champaign*),
Nicholas G. Edmonds, Andrew Lumsdaine (*Indiana University*)
- **Using Memory Mapping to Support Cactus Stacks in Work-Stealing Runtime Systems**411
I-Ting Angelina Lee, Silas Boyd-Wickizer, Zhiyi Huang,
Charles E. Leiserson (*Massachusetts Institute of Technology*)

Session 6B: Speculation

Session Chair: Jim Dehnert (*Google*)

- **Speculative-Aware Execution: A Simple and Efficient Technique for Utilizing Multi-Cores to Improve Single-Thread Performance**421
Rania H. Mameesh (*University of Siena, Italy*), Manoj Franklin (*University of Maryland in College Park*)
- **The Potential of Using Dynamic Information Flow Analysis in Data Value Prediction**431
Walid J. Ghandour, Haitham Akkary, Wes Masri (*American University of Beirut*)
- **Efficient Runahead Threads**443
Tanausú Ramírez, Alex Pajuelo (*Universitat Politècnica de Catalunya*),
Oliverio J. Santana (*Universidad de Las Palmas de Gran Canaria*), Onur Mutlu (*Carnegie Mellon University*),
Mateo Valero (*Universitat Politècnica de Catalunya*)
- **Energy Efficient Speculative Threads: Dynamic Thread Allocation in Same-ISA Heterogeneous Multicore Systems**453
Yangchun Luo (*University of Minnesota Twin Cities*), Venkatesan Packirisamy (*NVIDIA Corporation*),
Wei-Chung Hsu (*National Chiao Tung University*), Antonia Zhai (*University of Minnesota*)

Session 7A: Caches and Coherence II

Session Chair: Aamer Jaleel (*Intel*)

- **SWEL: Hardware Cache Coherence Protocols to Map Shared Data Onto Shared Caches**465
Seth H. Pugsley, Josef B. Spjut, David W. Nellans, Rajeev Balasubramanian (*University of Utah*)
- **ATAC: A 1000-Core Cache-Coherent Processor with On-Chip Optical Network**477
George Kurian, Jason E. Miller, James Psota, Jonathan Eastep, Jifeng Liu, Jurgén Michel,
Lionel C. Kimerling, Anant Agarwal (*Massachusetts Institute of Technology*)
- **Using Dead Blocks as a Virtual Victim Cache**489
Samira Khan, Daniel A. Jiménez (*The University of Texas at San Antonio*), Doug Burger (*Microsoft Research*),
Babak Falsafi (*Ecole Polytechnique Fédérale de Lausanne*)

Session 7B: Data Distribution and Tiling

Session Chair: Lawrence Rauchwerger (*Texas A&M University*)

- **Compiler-Assisted Data Distribution for Chip Multiprocessors**501
Yong Li, Ahmed Abousamra, Rami Melhem, Alex K. Jones (*University of Pittsburgh*)
- **Data Layout Transformation Exploiting Memory-Level Parallelism in Structured Grid Many-Core Applications**513
I-Jui Sung, John A. Stratton, Wen-Mei W. Hwu (*University of Illinois at Urbana-Champaign*)
- **Tiled-MapReduce: Optimizing Resource Usages of Data-Parallel Applications on Multicore with Tiling**523
Rong Chen, Haibo Chen, Binyu Zang (*Fudan University*)

Poster Session

Session Chair: Michael Franz (*University of California at Irvine*)

- **On-Chip Network Design Considerations for Compute Accelerators**535
Ali Bakhoda (*University of British Columbia*), John Kim (*Korea Advanced Institute of Science and Technology*),
Tor M. Aamodt (*University of British Columbia*)
- **Believe It Or Not! Multi-Core CPUs Can Match GPU Performance for a FLOP-Intensive Application!**537
Rajesh Bordawekar, Uday Bondhugula, Ravi Rao (*IBM T.J. Watson Research Center*)

• Ordered and Unordered Algorithms for Parallel Breadth First Search	539
M. Amber Hassaan, Martin Burtseher, Keshav Pingali (<i>University of Texas at Austin</i>)	
• Moths: Mobile Threads for On-Chip Networks	541
Matthew Mislser, Natalie Enright Jerger (<i>University of Toronto</i>)	
• Improving Speculative Loop Parallelization Via Selective Squash and Speculation Reuse ...	543
Santhosh S. Ananthramu, Deepak Majeti (<i>Rice University</i>), Sanjeev Kumar Aggarwal, Mainak Chaudhuri (<i>Indian Institute of Technology</i>)	
• Revisiting Sorting for GPGPU Stream Architectures	545
Duane G. Merrill, Andrew S. Grimshaw (<i>University of Virginia</i>)	
• Analyzing Cache Performance Bottlenecks of STM Applications and Addressing Them with Compiler's Help	547
Sandya S. Mannarswamy (<i>Indian Institute of Science and HP India</i>), R. Govindarajan (<i>Indian Institute of Science</i>)	
• An Intra-Tile Cache Set Balancing Scheme	549
Mohammad Hammoud, Sangyeun Cho, Rami G. Melhem (<i>University of Pittsburgh</i>)	
• StatCC: A Statistical Cache Contention Model	551
David Eklov, David Black-Schaffer, Erik Hagcrsten (<i>Uppsala University</i>)	
• An Integer Programming Framework for Optimizing Shared Memory Use on GPUs	553
Wenjing Ma, Gagan Agrawal (<i>The Ohio State University</i>)	
• Exploiting Subtrace-Level Parallelism in Clustered Processors	555
Rafael Ubal, Julio Sahuquillo, Salvador Petit, Pedro López, Jose Duato (<i>Universidad Politécnica de Valencia</i>)	
• A Case for NUMA-Aware Contention Management on Multicore Systems	557
Sergey Blagodurov, Sergey Zhuravlev, Alexandra Fedorova, Ali Kamali (<i>Simon Fraser University</i>)	
• DMATiler: Revisiting Loop Tiling for Direct Memory Access	559
Haibo Lin, Tao Liu (<i>IBM Research - China</i>), Huoding Li (<i>IBM Systems & Technology Group, China</i>), Tong Chen, Lakshminarayanan Renganarayanan, John Kevin O'Brien (<i>IBM T.J. Watson Research Center</i>), Ling Shao (<i>IBM Research - China</i>)	
• Scaling of the PARSEC Benchmark Inputs	561
Christian Bienia, Kai Li (<i>Princeton University</i>)	
• Online Cache Modeling for Commodity Multicore Processors	563
Richard West (<i>Boston University</i>), Puneet Zaroo, Carl A. Waldspurger (<i>VMware, Inc.</i>), Xiao Zhang (<i>University of Rochester</i>)	
• NoC-Aware Cache Design for Chip Multiprocessors	565
Ahmed K. Abousamra, Rami G. Melhem, Alex K. Jones (<i>University of Pittsburgh</i>)	
• A Software-SVM-Based Transactional Memory for Multicore Accelerator Architectures with Local Memory	567
Jun Lee, Sangmin Seo, Jaejin Lee (<i>Seoul National University</i>)	
• NUcache: A Multicore Cache Organization Based on Next-Use Distance	569
R. Manikantan (<i>Indian Institute of Science, Bangalore</i>), Kaushik Rajan (<i>Microsoft Research India</i>), R. Govindarajan (<i>Indian Institute of Science, Bangalore</i>)	
• CoreGenesis: Erasing Core Boundaries for Robust and Configurable Performance	571
Shantanu Gupta, Shuguang Feng, Amin Ansari, Ganesh Dasika, Scott Mahlke (<i>University of Michigan</i>)	
• Automatic Vector Instruction Selection for Dynamic Compilation	573
Rajkishore Barik, Jisheng Zhao, Vivek Sarkar (<i>Rice University</i>)	
• Approximating Age-Based Arbitration in On-Chip Networks	575
Michael M. Lee, John Kim (<i>Korea Advanced Institute of Science and Technology</i>), Dennis Abts, Michael Marty (<i>Google Inc.</i>), Jae W. Lee (<i>Parakinetics Inc.</i>)	
Author Index	577