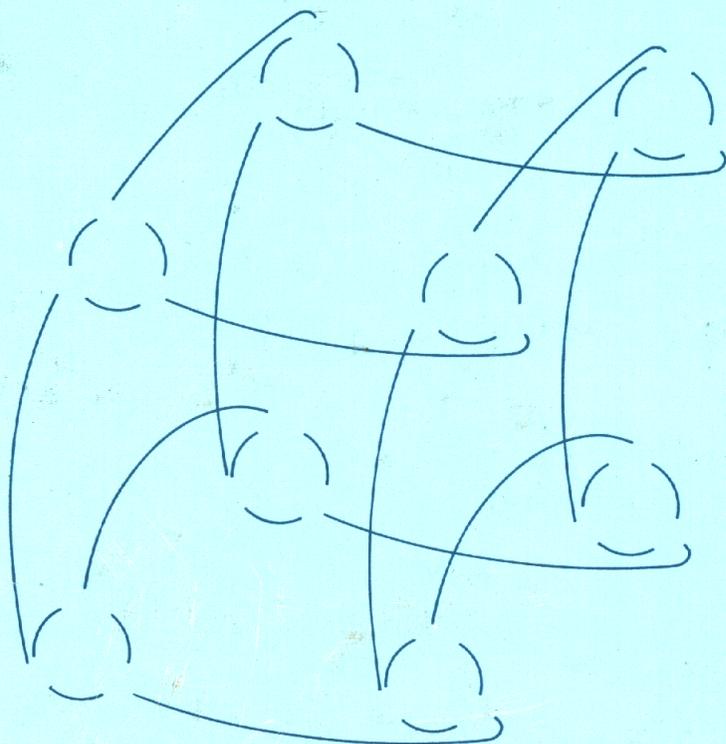


# COMPUTATIONAL ASPECTS OF VLSI

JEFFREY D. ULLMAN



COMPUTER SCIENCE PRESS

BIBLIOTHEQUE DU CERIST

C1630

**COMPUTATIONAL  
ASPECTS OF  
VLSI**

**JEFFREY D. ULLMAN**  
*STANFORD UNIVERSITY*

BIBLIOTHEQUE DU CERIST

COMPUTER SCIENCE PRESS

# TABLE OF CONTENTS

<b>Chapter 1: VLSI Models</b>	<b>1</b>
1.1: Integrated Circuits and the Mead-Conway Rules	1
1.2: VLSI Implementation of Logic	11
1.3: Electrical Properties of Circuits	18
1.4: Abstractions of VLSI Circuits	29
Exercises	38
Bibliographic Notes	40
<b>Chapter 2: Lower Bounds on Area and Time</b>	<b>42</b>
2.1: Introduction to Lower Bound Arguments	42
2.2: Information and Crossing Sequences	50
2.3: Probabilistic Circuits and Algorithms	58
2.4: Circuits with Repetition of Inputs	67
Exercises	75
Bibliographic Notes	78
<b>Chapter 3: Layout Algorithms</b>	<b>80</b>
3.1: H-trees	81
3.2: Lower Bounds on Tree Layouts	85
3.3: A Divide-and-Conquer Layout Algorithm	91
3.4: Layout of Regular Expression Recognizers	102
3.5: Layout of Planar Graphs	111
Exercises	127
Bibliographic Notes	130
<b>Chapter 4: Algorithm Design for VLSI</b>	<b>131</b>
4.1: Processors and Processor Networks	132
4.2: A Programming Language for Processors	139
4.3: The Tree-of-Processors Organization	143
4.4: The Mesh-of-Processors Organization	149
4.5: The Mesh-of-Trees Organization	158
Exercises	173
Bibliographic Notes	174

<b>Chapter 5: Systolic Algorithms</b>	<b>175</b>
5.1: Introduction: Systolic Convolution	175
5.2: Transformation Rules for Systolic Algorithms	178
5.3: Matrix Multiplication and Transitive Closure	189
5.4: Other Matrix and Graph Algorithms	198
Exercises	206
Bibliographic Notes	208
<b>Chapter 6: Organizations with High Wire Area</b>	<b>209</b>
6.1: The Shuffle-Exchange Organization	210
6.2: The Butterfly Organization	216
6.3: Algorithms on Butterfly Networks	219
6.4: Ideal Parallel Computers and Their Simulation	227
Exercises	241
Bibliographic Notes	242
<b>Chapter 7: Overview of VLSI Design Systems</b>	<b>244</b>
7.1: Design Languages	244
7.2: CIF: A Geometry Language	252
7.3: CHISEL: A Preprocessor for Generating CIF	258
7.4: Esim: A Switch Level Language	268
7.5: Lgen: A Logic Language	269
7.6: LAVA: A Sticks Language	273
7.7: PLA's and Their Personalities	283
7.8: Finite Automaton Languages: SLIM	290
7.9: A Regular Expression Language	300
Exercises	307
Bibliographic Notes	309
<b>Chapter 8: Compilation and Optimization Algorithms</b>	<b>310</b>
8.1: Optimization of PLA Personalities	311
8.2: Compilation of Sticks Languages	323
8.3: Compilation of Logic	338
8.4: Compilation of Regular Expressions	355
8.5: Toward Silicon Compilation	369
Exercises	378
Bibliographic Notes	380
<b>Chapter 9: Algorithms for VLSI Design Tools</b>	<b>382</b>
9.1: Reporting Intersections of Rectangles	382
9.2: Circuit Extraction Algorithms	393
9.3: Design Rule Checking	398

9.4: An Algorithm for Simulation of Switch Circuits	408
9.5: The PI Placement and Routing System	425
9.6: Optimal Routing	439
Exercises	450
Bibliographic Notes	453
<b>Appendix</b>	<b>455</b>
A.1: Big-Oh and Big-Omega	455
A.2: Depth-First Search	456
A.3: Regular Expressions and Nondeterministic Automata	457
A.4: Sketch of the Flashsort Parallel Sorting Algorithm	461
<b>Bibliography</b>	<b>466</b>
<b>Index</b>	<b>484</b>