



A Cost-Efficient Digital ESN Architecture on FPGA for OFDM Symbol Detection

VICTOR M. GAN, YIBIN LIANG, LIANJUN LI, LINGJIA LIU, and YANG YI,

Virginia Polytechnic Institute and State University

The echo state network (ESN) is a recently developed machine-learning paradigm whose processing capabilities rely on the dynamical behavior of recurrent neural networks. Its performance outperforms traditional recurrent neural networks in nonlinear system identification and temporal information processing applications. We design and implement a cost-efficient ESN architecture on field-programmable gate array (FPGA) that explores the full capacity of digital signal processor blocks on low-cost and low-power FPGA hardware. Specifically, our scalable ESN architecture on FPGA exploits Xilinx DSP48E1 units to cut down the need of configurable logic blocks. The proposed architecture includes a linear combination processor with negligible deployment of configurable logic blocks and a high-accuracy nonlinear function approximator. Our work is verified with the prediction task on the classical NARMA dataset and a symbol detection task for orthogonal frequency division multiplexing systems using a wireless communication testbed built on a software-defined radio platform. Experiments and performance measurement show that the new ESN architecture is capable of processing real-world data efficiently for low-cost and low-power applications.

CCS Concepts: • **Hardware** → **Hardware accelerators**; • **Computing methodologies** → **Neural networks**;

Additional Key Words and Phrases: Reservoir computing, echo state network, field-programmable gate array, digital signal processing, symbol detection, OFDM, wireless communication

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1 INTRODUCTION

The neural network has shown extraordinary effectiveness on a wide variety of applications, such as image recognition [38, 46], speech processing [16, 35], and wireless communication [48, 49]. With the great success in applications also comes the evolution of hierarchical neural network architecture. **The recurrent neural network (RNN)**, as a sub-category of the neural network,

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Authors' address: V. M. Gan, Y. Liang, L. Li, L. Liu, and Y. Yi, Virginia Polytechnic Institute and State University, 1185 Perry Street, Blacksburg, VA; emails: {victorgan, yibin, lianjunli, ljliu, yangyi8}@vt.edu.

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