A Control Theoretic Approach to Energy-Efficient Pipelined Computation in MPSoCs

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In this work, we describe a control theoretic approach to dynamic voltage/frequency scaling (DVFS) in a pipelined MPSoC architecture with soft real-time constraints, aimed at minimizing energy consumption with throughput guarantees. Theoretical analysis and experiments carried out on a cycle-accurate, energy-aware, and multiprocessor simulation platform are provided. We give a dynamic model of the system behavior which allows to synthesize linear and nonlinear feedback control schemes for the run-time adjustment of the core frequencies. We study the characteristics of the proposed techniques in both transient and steady-state conditions. Finally, we compare the proposed feedback approaches and local DVFS policies from an energy consumption viewpoint.

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