Resilient and Adaptive Performance Logic

BAO LIU, XUEMEI CHEN, and FIONA TESHOME, University of Texas at San Antonio

As VLSI technology continues scaling, increasingly significant parametric variations and increasingly prevalent defects present unprecedented challenges to VLSI design at nanometer scale. Specifically, performance variability has hindered performance scaling, while soft errors become an emerging problem for logic computation at recent technology nodes. In this article, we leverage the existing Totally Self-Checking (TSC)/Strongly Fault-Secure (SFS) logic design techniques, and propose Resilient and Adaptive Performance (RAP) logic for maximum adaptive performance and soft error resilience in nanoscale computing. RAP logic clears all timing errors in the absence of external soft errors, albeit at a higher area/power cost compared with Razor logic. Our experimental results further show that dual-rail static (Domino) RAP logic outperforms alternative Delay-Insensitive (DI) code-based static (Domino) RAP logic with less area, higher performance, and lower power consumption for the large test cases, and achieves an average of 2.29(2.41)× performance boost, 2.12(1.91)× layout area, and 2.38(2.34)× power consumption compared with the traditional minimum area static logic based on the Nangate 45-nm open cell library.

Categories and Subject Descriptors: B.6.2 [**Logic Design**]: Reliability and Testing; B.8.1 [**Performance and Reliability**]: Reliability, Testing and Fault-Tolerance

General Terms: Design, Reliability, Performance

Additional Key Words and Phrases: VLSI, reliability, performance

ACM Reference Format:
Liu, B., Chen, X., and Teshome, F. 2012. Resilient and adaptive-performance logic. ACM J. Emerg. Technol. Comput. Syst. 8, 3, Article 22 (August 2012), 16 pages.
DOI = 10.1145/2287696.2287705 http://doi.acm.org/10.1145/2287696.2287705

1. INTRODUCTION

As VLSI technology scales into the nanometer domain, VLSI systems are subject to increasingly prevalent catastrophic defects, soft errors, and significant parametric variations [Blish et al. 2003], which cannot be reduced below certain levels at nanometer scale according to quantum physics. They present unprecedented challenges to nanoscale VLSI design.

A specific challenge is to continue performance scaling. In today's synchronous VLSI designs, a clock cycle time is determined by the worst-case signal propagation path delay in the combinational logic. An increase in performance variability leads to an increase in clock cycle time or performance degradation. As a result, performance has stopped scaling in recent years, throughput becomes the primary goal in microprocessor design, and multicore architectures arise.

Another emerging challenge to VLSI design is soft errors. Soft errors have been a problem for space applications and modern memory systems [Elkind and Siewiorek

Authors' addresses: B. Liu (corresponding author), X. Chen, and F. Teshome, Electrical and Computer Engineering Department, University of Texas, San Antonio, TX; email: bliu@utsa.edu.

DOI 10.1145/2287696.2287705 http://doi.acm.org/10.1145/2287696.2287705