



# From Transistors to NEMS: Highly Efficient Power-Gating of CMOS Circuits

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A rapidly growing class of battery constrained electronic applications are those with very long sleep periods, such as structural health monitoring systems, biomedical implants, and wireless border security cameras. The traditional method for sleep-mode power reduction, transistor power gating, has drawbacks, including performance loss and residual leakage. This article presents a thorough evaluation of a new nanotechnology-enabled power gating structure, CMOS-compatible NEMS switches, in the presence of aggressive supply voltage scaling. Due to the infinite off-resistance of the NEMS switches, the average power consumption of an FFT processor performing 1 FFT per hour drops by around 30 times compared to a transistor-based power gating implementation. Additionally, the low on-resistance and nanoscale size means even with current prototypes, area overhead is as much as 5 times lower, with much room for improvement. The major drawback of NEMS switches is the high activation voltage, which can be many times higher than typical CMOS supply voltages. We demonstrate that with a charge pump, these voltages can be generated on-die, and the energy and bootup delay overhead is negligible compared to the FFT processing itself. These results show that NEMS-based power-gating warrants further investigation and the fabrication of a prototype.

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## 1. INTRODUCTION

As portable electronics become more embedded in the surrounding environment, the amount of time spent idle has increased dramatically, which has major implications on system design. Consider, for example, a structural health monitoring system that uses a piezoelectric pulse and an FFT to scan a building's health once a day [Kim et al. 2007]. Since the device has all day to perform the FFT, the target throughput is low and the performance constraints are very relaxed. The device will spend very little time active and a lot of time idle, so the static power dominates the total energy consumption. Other examples include multilevel sensor designs, where a more sophisticated sensor, e.g. a wireless smart camera, spends most of its time in a sleep mode, waiting to be awakened by a simple low level sensor [Ansari et al. 2009]. Regardless of their usage, a common characteristic of most low-throughput designs is that they have

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This work is an expansion of Henry and Nazhandali [2010].

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