A Torus-Based Hierarchical Optical-Electronic Network-on-Chip for Multiprocessor System-on-Chip

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Networks-on-chip (NoCs) are emerging as a key on-chip communication architecture for multiprocessor systems-on-chip (MPSoCs). Optical communication technologies are introduced to NoCs in order to empower ultra-high bandwidth with low power consumption. However, in existing optical NoCs, communication locality is poorly supported, and the importance of floorplanning is overlooked. These significantly limit the power efficiency and performance of optical NoCs. In this work, we address these issues and propose a torus-based hierarchical hybrid optical-electronic NoC, called THOE. THOE takes advantage of both electrical and optical routers and interconnects in a hierarchical manner. It employs several new techniques including floorplan optimization, an adaptive power control mechanism, low-latency control protocols, and hybrid optical-electrical routers with a low-power optical switching fabric. Both of the unfolded and folded torus topologies are explored for THOE. Based on a set of real MPSoC applications, we compared THOE with a typical torus-based optical NoC as well as a torus-based electronic NoC in 45nm on a 256-core MPSoC, using a SystemC-based cycle-accurate NoC simulator. Compared with the matched electronic torus-based NoC, THOE achieves 2.46X performance and 1.51X network switching capacity utilization, with 84% less energy consumption. Compared with the optical torus-based NoC, THOE achieves 4.71X performance and 3.05X network switching capacity utilization, while reducing 99% of energy consumption. Besides real MPSoC applications, a uniform traffic pattern is also used to show the average packet delay and network throughput of THOE. Regarding hardware cost, THOE reduces 75% of laser sources and half of optical receivers compared with the optical torus-based NoC.

Categories and Subject Descriptors: C.1.2 [**Processor Architectures**]: Multiple Data Stream Architectures (Multiprocessors)—*Interconnection architectures, Parallel processors*

General Terms: Design, Performance

Additional Key Words and Phrases: Hierarchical architecture, multiprocessor system-on-chip, optical network-on-chip, optical-electronic router, power consumption

ACM Reference Format:
Ye, Y., Xu, J., Wu, X., Zhang, W., Liu, W., and Nikdast, M. 2012. A torus-based hierarchical optical-electronic network-on-chip for multiprocessor system-on-chip. ACM J. Emerg. Technol. Comput. Syst. 8, 1, Article 5 (February 2012), 26 pages.
DOI = 10.1145/2093145.2093150 http://doi.acm.org/2093145.2093150

This work is partially supported by HKUST RPC and RGC of the Hong Kong Special Administrative Region, China.
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DOI 10.1145/2093145.2093150 http://doi.acm.org/10.1145/2093145.2093150