Design Considerations for Multilevel CMOS/Nano Memristive Memory

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With technology migration into nano and molecular scales several hybrid CMOS/nano logic and memory architectures have been proposed that aim to achieve high device density with low power consumption. The discovery of the memristor has further enabled the realization of denser nanoscale logic and memory systems by facilitating the implementation of multilevel logic. This work describes the design of such a multilevel nonvolatile memristor memory system, and the design constraints imposed in the realization of such a memory. In particular, the limitations on load, bank size, number of bits achievable per device, placed by the required noise margin for accurately reading and writing the data stored in a device are analyzed. Also analyzed are the nondisruptive read and write methodologies for the hybrid multilevel memristor memory to program and read the memristive information without corrupting it. This work showcases two write methodologies that leverage the best traits of memristors when used in either linear (low power) or nonlinear drift (fast speeds) modes. The system can therefore be tailored depending on the required performance parameters of a given application for a fast memory or a slower but very energy-efficient system. We propose for the first time, a hybrid memory that aims to incorporate the area advantage provided by the utilization of multilevel logic and nanoscale memristive devices in conjunction with CMOS for the realization of a high density nonvolatile multilevel memory.

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1. INTRODUCTION

Continued technology migration into the nanometer regime has led to the design of several hybrid CMOS/nano logic and memory architectures, each of which target high device density and low power consumption. Several methodologies to replace or extend CMOS technology have projected highly dense systems with low power consumption and little to no performance degradation [Bez and Pirovano 2004; DeHon 2003; Kim et al. 2009; Strukov and Likharev 2005]. The discovery of memristance in nanoscale metal-oxide devices [Chua 1971, 2008; Strukov and Williams 2008] has further broadened the scope of nanoscale architectures to implement nonconventional logic, while increasing memory and logic density [Rajendran et al. 2009; Snider 2008]. With an increasing necessity for larger and more compact digital data storage, alternative

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